ABSTRACT OF THE DISCLOSURE

HIGH PERFORMANCE IPSEC HARDWARE ACCELERATOR FOR PACKET CLASSIFICATION

Inventors:
Li-Jau (Steven) Yang
Chi-Li Wang
Kap Soh
Chin-Li (Karen) Mou

An architecture for a high performance IPSEC accelerator. The architecture includes components for scanning fields of packets, programming an IPSEC services device according to the scanned fields, and modifying the scanned packet with an output from the IPSEC security services device. Preferably, the architecture is implemented in hardware, and attached to a host machine. Hardware devices, fast in comparison to software processing and network speeds, allows the computationally intensive IPSEC processes to be completed in real-time and reduce or eliminate bottlenecks in the path of a packet being sent or received to/from a network.